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Pelican™ VME/PMC Carriers and ANSI/VITA 35-2000

Introduction

Sabtech's Pelican™ family of carrier products provides customers with a way to incorporate PCI Mezzanine Card (PMC) modules into systems that use other busses or PCI form factors. One of the most popular applications of PMC modules is to install them on VME carrier boards or single board computer (SBC or CPU) boards and use them in VME systems.

Confusion often arises when user I/O signals are routed between PMC modules and the VME bus. There are a variety of ways the signals can be routed, and often the end user is left with the task of determining if a particular VME/PMC carrier board will support the necessary user I/O routing for a specific PMC module.

This document will help end users understand the differences in user I/O routing, and will help the user in determining which Sabtech Pelican™ VME/PMC carrier is right for the job.

Background

PMC modules have been around since about 1995, even though the IEEE specification defining PMC modules was not ratified until 2001. IEEE 1386 defines the Common Mezzanine Card family, and IEEE 1386.1 defines the Physical and Environmental Layers for PCI Mezzanine Cards.

PMC modules come in different sizes. There are single-wide and double-wide modules. There are also extended modules, which are longer than the non-extended modules. The majority of PMC modules manufactured are single-wide non-extended modules. These modules have 4 connectors, which have reference designators P11, P12, P13, and P14. Often, the middle '1' is dropped, and the connectors carry reference designators of P1, P2, P3, and P4. Each of the connectors has 64 pins.

Boards that carry PMC modules are called “host” boards. On the host board, the mating PMC connectors carry reference designators of Jn1, Jn2, Jn3, and Jn4. The 'n' refers to the PMC “slot.” Most VME carrier boards provide two PMC slots, so the PMC connectors on these host boards have reference designators of J11, J12, J13, and J14 for PMC slot 1, and J21, J22, J23, and J24 for PMC slot 2.

Pn1/Jn1, Pn2/Jn2, and Pn3/Jn3 connectors are reserved for PCI bus signals. Pn4/Jn4 is reserved for user I/O, and can be used for any arbitrary user defined signaling. PMC manufacturers often use the user I/O signals for application specific signals.

The VME bus also provides several user I/O signals on the VME P2 connector. With the ratification of ANSI/VITA 1-1994 and ANSI/VITA 1.1-1997, more user I/O pins were defined on the 5-row VME P2 connector, and additionally on the VME P0 connector.

In the absence of any standard governing the routing of PMC user I/O signals to VME User I/O signals, several manufacturers drafted their own proprietary mappings. Motorola, V-Metro, and Themis, are some of the companies that came up with their own mappings. It wasn't until ANSI/VITA 35-2000 was ratified that there was a governing standard for routing PMC User I/O to VME User I/O.

ANSI/VITA 35-2000

ANSI/VITA 35-2000 defines 4 different mappings. Section 2.2 defines mapping a single PMC P4 to VME-P0 mapping, section 2.3 defines mapping a single PMC P4 to VME P2 rows A and C, section 2.4 defines mapping a single PMC P4 to VME64x P2 rows D and Z, and section 2.6 defines mapping two PMC P4's to VME P2 rows A and C.

Before continuing, the following should be understood. Each PMC connector has 64 pins, which means that each PMC P4 connector has 64 User I/O signals.

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The standard VME P2 connector has 3 rows, A, B, and C, each of which has 32 pins. Only rows A and C are defined as User I/O, so there are a total of 64 User I/O pins on a standard VME P2 connector.

VME64x P2 connectors have 5 rows; Z, A, B, C, and D. Row D provides only 30 additional pins for User I/O. Pin 31 is defined as a Voltage Pre-Charge pin (VPC), and pin 32 is Ground. Every other pin in Row Z is Ground, so Row Z provides only an additional 16 pins. All together, with the addition of two more rows to the VME P2 connector, only 46 addition user defined I/O pins were gained.

The VME P0 connector provides 5 more rows of 19 pins each, or a total of 95 additional User I/O pins.

With this information, and with the knowledge that not all VME systems are VME64x compliant, meaning they don't have P0 or 5-row P2 connectors, the dilemma of how to map all of the user I/O pins from two PMC modules begins to come into focus. There aren't enough pins to map all 64 pins from two PMC P4 connectors to the VME P2 connector. Even with a VME64x P2 connector, there are still only 110 pins available; 128 are needed. So, trade-offs must be made in determining how a particular carrier board will be designed so it can provide the maximum flexibility to the target customer base.

Mapping a single PMC P4 to VME P0 provides 64 user I/O signals. Host boards that map one of the PMC P4 connector pins to P0 in accordance with ANSI/VITA 35-2000 section 2.2 are said to be “P4V0-64” compliant. However, this mapping does not apply to non-VME64x systems.

Mapping a single PMC-P4 to VME P2 Rows A and C provides 64 user I/O signals. Host boards that map one of the P4 connectors to P0 in accordance with ANSI/VITA 35-2000 section 2.3 are said to be “P4V2-64ac” complaint. However, this uses all of the available User I/O pins for non VME64x system. For host boards that can carry two or more PMC modules, there are no pins for user I/O from the other PMC module.

Mapping a single PMC P4 to VME64x Rows D and Z provides 46 user I/O signals. Host boards that map one of the P4 connectors to VME64x P2 in accordance with ANSI/VITA 35-2000 section 2.4 are said to be “P4V2-46dz” compliant. However, this are not enough pins for all of the user I/O from one PMC module, so if the additional I/O is needed, it would have to be mapped to VME64x P2 Rows A and C. For board that carry two PMC modules, this causes a problem because some of the user I/O pins for the 2nd PMC module will be used.

And finally, mapping dual PMC P4 connectors to VME P2 Rows A and C provides 32 pins from each of the PMC P4 connectors. Host boards that are mapped in accordance with ANSI/VITA 35-2000 section 2.5 are said to be “P4V2-32+32ac” compliant. However, the obvious problem is that not all of the User I/O pins from the P4 connectors are mapped.

Pelican Variations

In order to address all of these problems, and to provide customers with a product that can meet any of the requirements defined in ANSI/VITA 35/2000, there are three different Sabtech Pelican™ VME/PMC Carriers; The Pelican™ VME/PMC, the Pelican64™ VME/PMC, and the Pelican64x™ VME/PMC.

The Pelican™ VME/PMC Carrier can be P4V2-46dz compliant, or P4V2-64ac compliant, but not both at the same time. The reason is that in addition to the ANSI/VITA 35-2000 mapping, the Pelican™ VME/PMC Carrier was designed to be complaint with existing carrier board products. As such, 18 of the User I/O pins are shared on VME P2 Rows A and C. This means is that all 64 User I/O pins of either one of the PMC modules is accessible, if only one of the cards is installed. However, 18 of the User I/O pins from P14 are connected to P24. The diagram below illustrates the Pelican™ VME/PMC Carrier I/O mapping. Note the purple area where the User I/O pins are shared.

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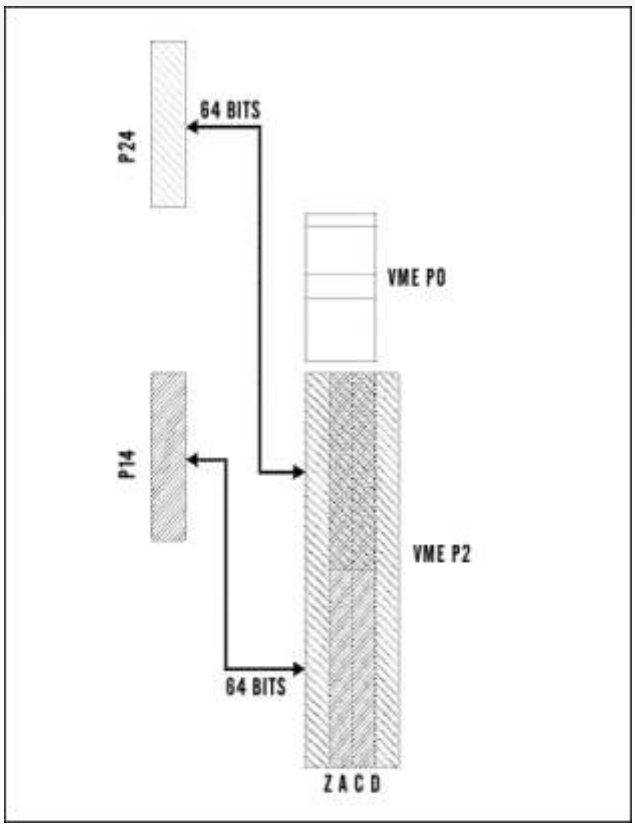

Figure 1: Pelican™ VME/PMC Carrier I/O Mapping

The Pelican64™ is P4V2-46dz compliant, and P4V2-32+32ac compliant. This means that in a VME 3-Row P2 system, 32 bits from each of the PMC P4 connectors is accessible simultaneously. It also means that 46 bits from P24 are accessible at the same time. Note that 32 of the 46 bits are the same as what is accessible on rows A and C. This card can be manufactured with three row connectors, and is the only board that should be used in VME 3- Row P2 systems. The diagram below illustrates the Pelican64™ VME/PMC Carrier I/O mapping.

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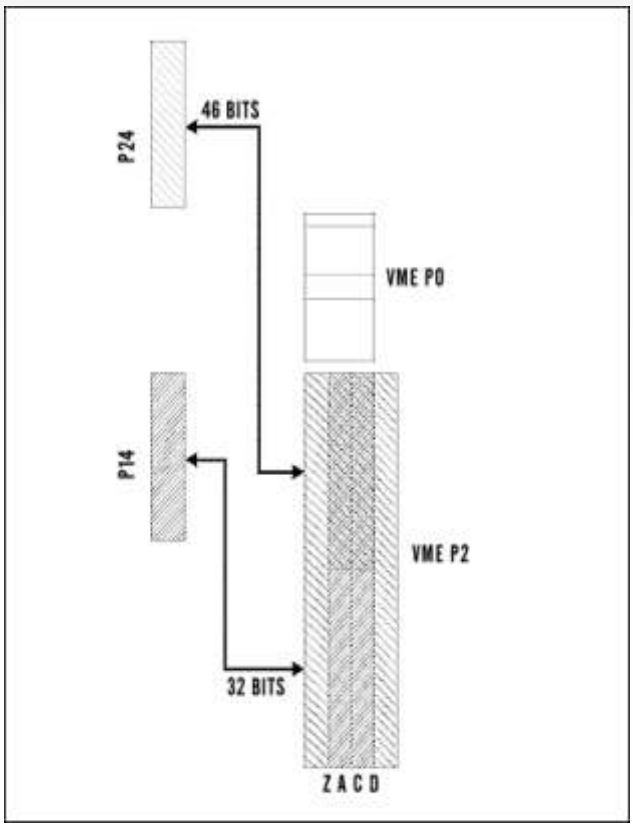

Figure 2: Pelican64™ VME/PMC Carrier I/O Mapping

The Pelican64x™ is P4V0-64 complaint and P4V2-64ac compliant. This means that all 64 bits from both PMC P4 connectors is accessible simultaneously. The figure below illustrates the Pelican64x™ VME/PMC Carrier I/O Mapping.

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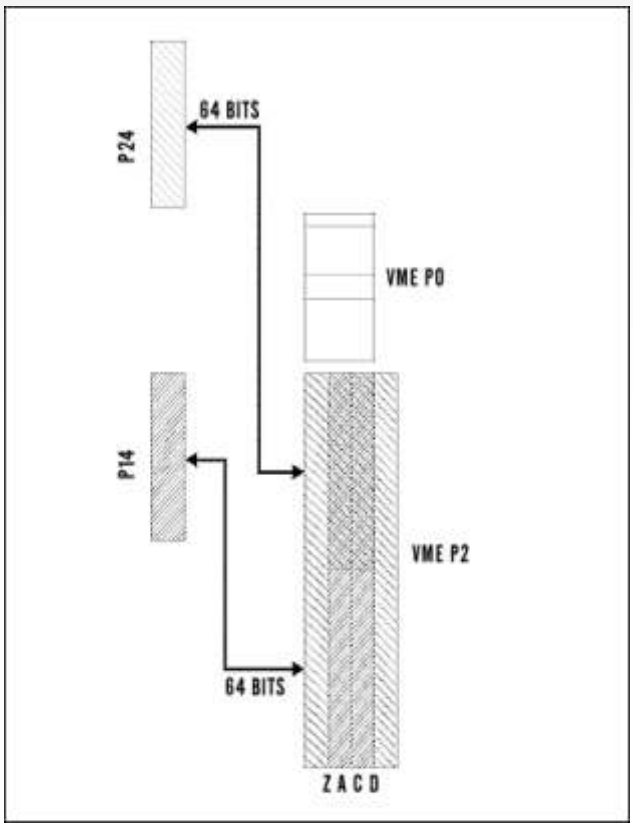

Figure 3: Pelican64x™ VME/PMC Carrier I/O Mapping

In addition to the figures, the following table can help users in determining which Pelican™ is needed for a particular application.

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35-2000 Section	From Connector	To Connector	Compliance Mnemonic	Pelican™ VME/PMC	Pelican64™ VME/PMC	Pelican64x™ VME/PMC
2.2	PMC-P4	VME-P0 (64 Bits)	P4V0-64			X
2.3	PMC-P4	VME-P2-Rows-A, C (64 bits)	P4V2-64ac	X*		X
2.4	PMC-P4	VME64x-P2-Rows-D, Z (46 bits)	P4V2-46ac	X*	X	
2.5	Dual PMC-P4	VME-P2- Rows-A, C (64 bits from each PMC-P4, 128 bits total)	P4V2-32+32ac		X	

*Mutually Exclusive

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